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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,854	09/25/2003	Stefan Bader	5367-42	9645

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EXAMINER	
TRAN, MINH LOAN	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,854	BADER ET AL.	
	Examiner	Art Unit	
	Minh-Loan T. Tran	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *3-5, 12, 24-45* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-11 and 13-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al. (6,531,719).

With regard to claim 1, figures 11 and 12 of Shibata et al. disclose a semiconductor chip 50 which emits electromagnetic radiation having an epitaxially produced semiconductor stack (16,17,18) based on nitride semiconductor material, which includes an n-GaN layer 16, a p-GaN layer 18, and an electromagnetic radiation generating region 17 which is arranged between these two semiconductor layers 16, 18; a base layer (15,11) on which the semiconductor stack (16, 17, 18) is arranged; and a TiN mirror layer 25 which is arranged between the semiconductor layer stack (16,17,18) and the base layer (15,11) and reflects electromagnetic radiation emitted by the semiconductor stack (16,17,18) in the direction of the base layer (15,11); wherein the mirror layer 25 has a plurality a planar reflection sub-surfaces which are positioned obliquely with respect to a main plane of the radiation-generating region 17 and each form an angle with respect to the main plane of the radiation-generating region 17.

Figures 11 and 12 of Shibata et al. do not disclose each of the planar reflection sub-surfaces of the mirror 25 forms an angle of between 10° and 50° with respect to the

main plane of the radiation-generating region 17. However, it would have been obvious to one of ordinary skill in the art to recognize that each planar reflection sub-surface of the mirror 25 of Shibata et al. forms an angle of between 10° and 50° with respect to the main plane of the radiation-generating region 17, because the mirror 25 having inclined faces that is formed as a texture structure that shape like teeth of a saw (note lines 5-13 in column 2 of Shibata et al.)

With regard to claim 6, figure 11 of Shibata et al. shows the mirror 25 having the reflection sub-surfaces form pyramid-like structures.

With regard to claim 21, Applicant's claim 21 does not distinguish over the Shibata et al. reference regardless of the process used to form the semiconductor chip because only the final product is relevant, not the process of making such as "a growth substrate wafer is at least partially removed after the epitaxially produced semiconductor stack has been grown."

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "

product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claim 22, lines 44-47 in column 4 of Shibata et al. disclose the p-type semiconductor layer is doped with magnesium (Mg).

With regard to claim 23, lines 25-32 in column 4 of Shibata et al. disclose the base (15,11) contains gallium arsenide.

Claims 2, 7-11, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al. (6,531,719).

With regard to claim 2, figure 11 of Shibata et al. discloses all the subject matter claimed except for the p-conducting semiconductor layer faces the base and the mirror is formed by means of a reflection surface of the p-conducting semiconductor layer. However, it would have been obvious to one of ordinary skill in the art to replace the n-type layer 16 of Shibata et al. to the p-type layer, and the p-type layer 18 of Shibata et al. to the n-type layer because the n-type layer and the p-type layer can be interchanged. Note figures 8 and 17 of Hosoba et al. are cited to support for the well known position. Further, Applicant's claim 2 does not distinguish over the Shibata et al. reference regardless of the process used to form the mirror layer because only the final product is relevant, not the process of making such as "the mirror layer (40) is formed by means of a reflection surface (131) of the p-conducting semiconductor layer (13)".

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re

Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

With regard to claims 7-11, figure 11 of Shibata et al. does not show the mirror layer 25 having a plurality of different layers such as highly reflective layer, a protective layer and a joining layer. However, it would have been obvious to one of ordinary skill in the art to form the mirror layer of Shibata et al. having a plurality of different layers such as highly reflective layer, a protective layer and a joining layer in order to obtain a maximum efficiency of the emitted light.

With regard to claims 19 and 20, figure 11 of Shibata et al. shows the transparent electrode 19 is formed on the p-GaN layer 18, but it does not show the transparent electrode is formed on the n-type layer. However, it would have been obvious to one of ordinary skill in the art to replace the n-type layer 16 of Shibata et al. to the p-type layer, and the p-type layer 18 of Shibata et al. to the n-type layer because the n-type layer and the p-type layer can be interchanged. Note figures 8 and 17 of Hosoba et al. are cited to support for the well known position. Further, it would have been obvious to one of ordinary skill in the art to form the transparent electrode layer of Shibata et al. that is

made of ITO or ZnO because such material is conventional in the art for forming the radiation-transmitting electrically conductive contact layer.

Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shibata et al. (6,531,719) in view of Shibata et al. (6,342,404).

With regard to claims 13 and 18, figures 1, 2, 11 of Shibata et al. ('719) do not show the semiconductor stack (16,17,18) includes at least one trench which defines a plurality of individual semiconductor layer elements. However, figures 1E, 2, 3, 6 of Shibata et al. ('404) shows the GaN semiconductor stack (26,27,28) includes at least one trench that is filled with an electrically insulating material 6 which transmits radiation generated by the radiation generating region 17; wherein the electrically insulating material 6 defines a plurality of individual semiconductor layer elements 5 (or 22). It would have been obvious to one of ordinary skill in the art to form the semiconductor stack (16,17,18) of Shibata et al. ('719) includes at least one trench which defines a plurality of individual semiconductor layer elements such as taught by Shibata et al. ('404) in order to simplify the processing steps of forming a plurality of light emitting devices.

With regard to claim 14, figures 1E, 2 and 3 of Shibata et al. ('404) show a plurality of trenches that are filled with electrically insulating material 6 extends in such a manner that the semiconductor layer elements 5 (or 22), in plan view, are in the shape of a quadrilateral.

With regard to claim 15, figure 11 of Shibata et al. ('719) shows the semiconductor layer elements 50 each has a width which includes at most 10 pyramid-like structures at the mirror layer 25.

With regard to claim 16, figure 6 of Shibata et al. ('404) shows the trenches that are filled with electrically insulating material 6 are at least sufficiently deep for them to isolate at least the radiation generating region 17.

With regard to claim 17, figures 1E and 6 of Shibata et al. ('404) do not disclose the width of the trenches that are filled with electrically insulating material 6 is at least double the depth of the trenches. However, it would have been obvious to one of ordinary skill in the art to form the width of the trenches Shibata et al.'s reference that are filled with electrically insulating material 6 is at least double the depth of the trenches, in order to ensure that the semiconductor layer elements 5 (or 22) are isolated.

Response to Arguments

2. Applicant's arguments, see remarks, filed 5/06/2005, with respect to the rejection(s)of claim(s) 1, 2, 6-11, 13-23 under 35 U.S.C. 102 (a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Shibata et al. (6,531,719) and Shibata et al. (6,342,404). This action is not made final.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh-Loan T. Tran whose telephone number is (571) 272-1922. The examiner can normally be reached on Monday-Friday 9:00 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mlt
06/2005

Minh-Loan T. Tran
Primary Examiner
Art Unit 2826